THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 52

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOJI SAKUI,
TAKEHIRO HASEGAWA, SHIGEYOSHI WATANABE,
FUJIO MASUOKA, TSUNEAKI FUSE, TOSHIKI SESHITA,
SEIICHI ARITOME, AKIHIRO NITAYAMA,
and FUMIO HORIGUCHI

Appeal No. 1997-3444
Application 08/268,728[1]

HEARD: July 12, 2000

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[1] Application for patent filed June 30, 1994, entitled (as amended in Paper No. 21) "Semiconductor Device Including A Bipolar Transistor Biased To Produce A Negative Base Current By The Impact Ionization Mechanism," which is a continuation of Application 08/035,205, filed March 22, 1993, now abandoned, which is a continuation of Application 07/660,982, filed February 27, 1991, now abandoned, which is a continuation of Application 07/293,807, filed January 5, 1989, now abandoned.

Before HAIRSTON, BARRETT, and BARRY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 21-31 and 35. Claims 36 and 37 have been withdrawn from consideration as directed to a non-elected invention.

We reverse.

BACKGROUND

The disclosed invention is directed to a semiconductor device including a bipolar transistor operating based on the reverse base current (RBC) effect discovered by Appellants to exist in the bipolar transistor.

Claim 21 is reproduced below.[2]

> 21. A semiconductor device comprising:
>
> a bipolar transistor having a base, an emitter, a collector, a base-emitter junction and a collector-base junction, said bipolar transistor having a first operating region such that with a positive base-emitter voltage V_{BE} in a first range and a predetermined positive

[2] In claim 21, as amended in Paper No. 36, "V_{BE}" has been miscopied from the amendment of Paper No. 21 as "VBE" in two places. This should be corrected because the claims will be printed from this amendment.

collector-emitter voltage V_{CE}, a positive base current I_B is produced, a second operating region such that with a positive base-emitter voltage V_{BE} in a second range greater than the first range and said positive collector-emitter voltage V_{CE}, a negative base current I_B is produced, said positive base-emitter voltage V_{BE} being determined so that said negative base current I_B is produced by impact ionization in said second operating region without actual breakdown, and a third operation region such that with a positive base-emitter voltage V_{BE} in a third range greater than the second range and said positive collective-emitter [sic, collector-emitter] voltage V_{CE}, a positive base current I_B is produced; and

means for biasing the bipolar transistor to operate with the positive collector-emitter voltage V_{CE} and at a boundary point between the second and third operation regions, including means for varying a voltage applied to the base of said bipolar transistor so that when V_{BE} exceeds a predetermined threshold and the voltage applied to the base of the bipolar transistor is removed by said means for biasing, the transistor is self-latched at the boundary between the second and third operating regions to output from the base of the bipolar transistor an output voltage at a first level, and so that when the voltage applied to the base of said bipolar transistor is such that V_{BE} is less than said threshold and said applied voltage is then removed by said means for biasing, the bipolar transistor operates in said first operating region and outputs from the base an output voltage at a second level different than said first level.

The Examiner relies on the following prior art:

Smith	3,538,349	November 3, 1970
Mar	3,727,076	April 10, 1973
Ando	4,134,032	January 9, 1979

Tsukada[3] 52-006036 January 18, 1977
(Japanese Published Unexamined Patent Application (Kokai))

Switching Transistor Handbook (1st ed., Motorola, Inc. 1963), pp. 29-67, 285-304 (hereinafter "Handbook")

Claims 21 and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the Handbook.

Claims 21, 22, and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tsukada.

Claims 21-24 and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Smith.

Claims 21-23, 25-28, 30, 31, and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ando.

Claims 21, 29, and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Mar.

We refer to the Final Rejection (Paper No. 32) and the Examiner's Answer (Paper No. 43) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 42) (pages referred to as "Br__") for a statement of Appellants' arguments thereagainst. The Reply

[3] Our understanding of this reference is based upon a translation prepared by the Patent and Trademark Office, a copy of which accompanies this decision.

Brief (Paper No. 46) has been denied entry as untimely (Paper No. 48), and is not considered.

OPINION

Objection to specification

While the objection to the specification is not within our jurisdiction, we advise the Examiner to consider withdrawing the rejection. The complete specification will provide more information to the public sooner than one that has been redacted.

Anticipation

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Handbook

The underlying question seems to be whether the reverse base current (RBC) effect described and claimed by Appellants is the same physical mechanism as latch-up in the avalanche breakdown region shown in the Handbook, just described in a

different way. The Examiner takes the position that operation of a bipolar transistor in the avalanche region as shown in the Handbook (pages 42 and 63-64) inherently meets the terms of the claims because there are two stable states, one of which is a stable point in the avalanche region called latch-up (page 64), and which is caused by impact ionization (page 65).

There is some evidence of record that RBC and classical bipolar snapback having a latch-up condition represent the same physical mechanism. See Hayden et al., A Comparison of Base Current Reversal and Bipolar Snapback in Advanced n-p-n Bipolar Transistors, IEEE Electron Device Letters, Vol. 12, No. 8, August 1991, pp. 407-409 (Paper 11 in Exhibit 2 filed with the Preliminary Amendment to predecessor Application 08/035,205, Paper No. 6); Ishimaru et al., A Reverse Base Current under High Level Injection, IEDM, 1991, pp. 91-865 to 91-868, at 91-865 (right col. description of Figure 2: "A snapback phenomenon was observed, which is caused by the existence of the reverse base current.") (Paper 13 in Exhibit 2 filed with the Preliminary Amendment to predecessor Application 08/035,205, Paper No. 6).

It is impossible for us to make a direct comparison between the mechanisms because the RBC is described in terms of base-emitter voltage V_{BE} and collector-emitter voltage V_{CE} as independent variables (figure 4), whereas the avalanche mode is described in terms of a family of curves of collector-emitter voltage V_{CE} versus collector current I_C for base currents I_B with no mention of V_{BE} (Handbook, figure 3-15). It does appear that there is a difference in operation, as disclosed, because in the RBC device, stable states both have $I_B = 0$ (the voltage to the base is removed), whereas in the avalanche mode, one state is for $I_B = 0$ and one state is $I_B < 0$ (i.e., I_{BR} or I_B(Reverse)). Also, the avalanche mode description in the Handbook does not describe a region of reverse base current (negative resistivity) between two regions of positive base current. Further, the stable states in figure 9-5b of the Handbook occur for a constant current of about 1 mA, whereas Appellants' device has different base current values as a function of V_{BE}. Still further, we agree with Appellants' argument that claim 21 requires a constant collector-emitter voltage V_{CE} (Br16) and the latching action in the Handbook does not take place at a constant V_{CE}. We

approach the rejection as a burden of proof issue. It is the Examiner's duty to make a prima facie case that what is claimed is inherent in the Handbook (and the other references). See In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138 (Fed. Cir. 1986).

It is the Examiner's position that all bipolar transistors are inherently capable of having the three operation regions recited in claim 21. Appellants apparently agree because no special bipolar transistor structure is required for operation; it is apparently only required that V_{CE} is high enough (compare figure 4, for V_{CE} = 6.25 V, to figure 6, for V_{CE} = 1 V). However, claim 21 calls for more than just a bipolar transistor having inherent operational characteristics. Assuming that all bipolar transistors are inherently capable of having the three operation regions recited in claim 21, the question is whether the Examiner has established that the circuit disclosed in the Handbook inherently has "means for biasing," "means for varying a voltage," and operates as recited in claim 21.

The Examiner states that figure 3-1 of the Handbook shows "a semiconductor device comprising: 'a bipolar transistor';

and 'means for biasing (V_{CC}, R_C, V_{BB} and R_B)' including a 'means for varying (V_{BB} and R_B)', all connected and operating similarly as recited by Applicant" (EA3). This statement is conclusory and makes no attempt to show how the circuit operates as claimed. Figure 3-1 is a general transistor circuit showing leakage currents that can operate in all modes depending on the bias conditions. Because it is necessary to provide some motivation to operate the circuit in a certain way, this circuit is not an anticipation. See In re Mills, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990) ("While Mathis' apparatus may be capable of being modified to run the way Mills' apparatus is claimed, there must be a suggestion or motivation in the reference to do so."). Nevertheless, since figures 2-17 (page 42) and 9-5a (page 291) show circuits for avalanche mode operation, we analyze these circuits.

The Examiner finds "[t]he fact that the reference teaches the exact operation presently claimed, whether in the positive or negative, can only be seen to be anticipation of the invention" (EA6) and "the mere fact that this reference teaches the 'latch-up' phenomenon can only be seen by one

skilled in the art as a direct anticipation of the claimed invention, whether the reference suggests using such operation or avoiding it" (EA6-7).

The fact that the transistor in the Handbook has a "latch-up" region of operation is not sufficient evidence to prove inherency of the specific operations in claim 21. First, the Examiner has not shown the existence of "a boundary point between the second and third operation regions" in the Handbook. It is not even apparent where the three regions could be in the diagrams showing the avalanche region, such as figure 3-15, because the diagrams are not defined in terms of V_{BE}.

Second, the Examiner has not shown how the Handbook anticipates the limitation of "means for biasing . . . including means for varying a voltage applied to the base of said bipolar transistor so that when V_{BE} exceeds a predetermined threshold and the voltage applied to the base of the bipolar transistor is removed by said means for biasing, the transistor is self-latched at the boundary between the second and third operating regions to output from the base of the bipolar transistor an output voltage at a first level."

The means for biasing operates in a specifical manner: the voltage is applied to the base and is then removed, leaving the transistor self-latched (see Appellants' figures 8 and 9). The biasing circuits of the Handbook do not remove the bias, as claimed. The Examiner has not shown that the transistor is latched at the boundary between the second and third operating regions, as defined in claim 21; mere latching in the Handbook is not sufficient to prove this condition. Further, the limitation requires the output to be at the base of the transistor, which is not the case in the Handbook.

Third, the Examiner has not shown how the Handbook anticipates the limitation "so that when the voltage applied to the base of said bipolar transistor is such that V_{BE} is less than said threshold and said applied voltage is then removed by said means for biasing, the bipolar transistor operates in said first operating region and outputs from the base an output voltage at a second level different than said first level." Again, the biasing circuits in the Handbook do not remove the bias and the output is not at the base of the transistor. Also, the Examiner has not shown that the

transistor operates in a first operating region, as that region has been claimed.

Fourth, Appellant argues that claim 21 requires a constant collector-emitter voltage V_{CE} and the latching action in the Handbook does not take place at a constant V_{CE} (Br16). The Examiner disagrees (EA8). We interpret claim 21 to require, by its consistent reference to "said positive collector-emitter voltage V_{CE}," the same collector-emitter voltage V_{CE} be maintained upon varying V_{BE}. The latching in the Handbook does not occur at a constant V_{CE} and, thus, it cannot be found that the claimed circuit operation is anticipated by the Handbook.

Because the Examiner has failed to carry his burden of proof to show inherency of the limitations of claim 21 in the Handbook, the anticipation rejection of claims 21 and 35 is reversed.

Tsukada

Appellants argue that Tsukada does not teach the biasing means and operation recited in claim 21 (Br17).

The Examiner finds that Tsukada has a transistor and means for biasing including a means for varying "all connected and operating similarly as recited by Applicant" (EA3) and contends that "all the regions of operation recited in the claims must inherently exist" (EA10).

The Examiner fails to show how the means for biasing, means for varying a voltage, and the operations in claim 21 are inherent in the structure of Tsukada. The fact that the transistor in the Tsukada is an avalanche transistor having a "latch" mode and is used as a memory element is not, by itself, sufficient to prove inherency of the specific structure and operations in claim 21. For example, the Examiner has not shown that Tsukada is inherently "self-latched at the boundary between the second and third operating regions," as claimed, or that the second state is in "said first operating region," as claimed. Moreover, it is clear that the memory states are stored in Tsukada at the collector (translation, page 4) and not at the base, as claimed.

Because the Examiner has failed to carry his burden of proof to show inherency of the limitations of claim 21 in

Tsukada, the anticipation rejection of claims 21, 22, and 35 is reversed.

Smith

The Examiner finds that Smith has a transistor and means for biasing including a means for varying "all connected and operating similarly as recited by Applicant" (EA4) and "that since the transistor operation claimed by Applicant is inherent to all bipolar transistors and since the reference can utilize any reasonable biasing, clearly the circuit to Smith would have such operation" (EA4).

As discussed in connection with the Handbook and Tsukada, inherency of the claimed subject matter is not established by a transistor and a bias circuit. We have reviewed Smith and do not see how it inherently discloses the claimed subject matter. Moreover, the Examiner's statement about "reasonable biasing" suggests that the circuit is only "capable of" being biased to operate as claimed. This is improper reasoning for an anticipation rejection. See Mills, 916 F.2d at 682, 16 USPQ2d at 1432. Because the Examiner has failed to carry his burden of proof to show inherency of the limitations of

claim 21 in Smith, the anticipation rejection of claims 21-24 and 35 is reversed.

Ando

The Examiner finds that Ando has a transistor and means for biasing including a means for varying "all connected and operating similarly as recited by Applicant" (EA4) and "that since the transistor operation claimed by Applicant is inherent to all bipolar transistors and since the reference can utilize any reasonable biasing, clearly the circuit to Ando would have such operation" (EA4).

As discussed in connection with the Handbook and Tsukada, inherency of the claimed subject matter is not established by a transistor and a bias circuit. We have reviewed Ando and do not see how it inherently discloses the claimed subject matter. Moreover, the Examiner's statement about "reasonable biasing" suggests that the circuit is only "capable of" being biased to operate as claimed. This is improper reasoning for an anticipation rejection. Id. Because the Examiner has failed to carry his burden of proof to show inherency of the

limitations of claim 21 in Ando, the anticipation rejection of claims 21-23, 25-28, 30, 31, and 35 is reversed.

Mar

The Examiner finds that Mar has a transistor and means for biasing including a means for varying "all connected and operating similarly as recited by Applicant" (EA4).

As discussed in connection with the Handbook and Tsukada, inherency of the claimed subject matter is not established by a transistor and a bias circuit. We have reviewed Mar and do not see how it inherently discloses the claimed subject matter. Because the Examiner has failed to carry his burden of proof to show inherency of the limitations of claim 21 in Ando, the anticipation rejection of claims 21, 29, and 35 is reversed.

CONCLUSION

The rejections of claims 21-31 and 35 are reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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